(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: 0 091 079
A3

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 83103132.3

(22) Date of filing: 29.03.83

(51) Int. Cl.³: H 01 L 29/78
H 01 L 29/08

(30) Priority: 01.04.82 JP 54485/82

(43) Date of publication of application:
12.10.83 Bulletin 83/41

(88) Date of deferred publication of search report: 23.11.83

(84) Designated Contracting States:
DE FR GB

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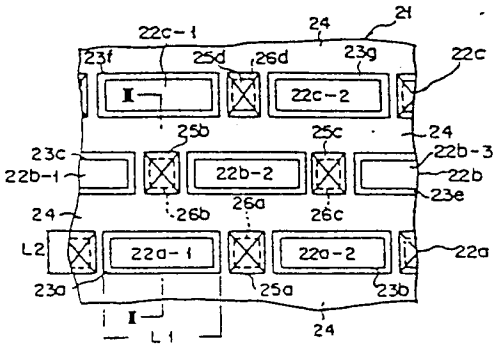
(54) Power MOSFET.

(57) A plurality of drain projections (22a-1, 22a-2, ...) are formed on a surface of a semiconductor substrate (21) in column and row directions. A portion is formed between two longitudinally adjacent drain projections (22a-1, 22a-2) so as to form a source electrode contact. A drain projection (22b-2) which is formed alongside the longitudinally adjacent drain projections (22a-1, 22a-2) is offset therefrom by a length corresponding to half of a long side of each projection.

FIG. 2



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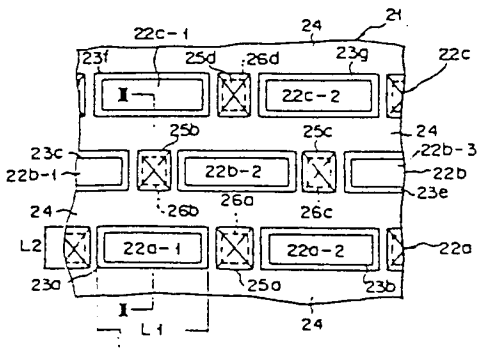

EP 0 091 079 A2

Power MOSFET

The present invention relates to a semiconductor device and, more particularly, to a power MOSFET.

A conventional power MOSFET has a plurality of independent source regions through a base region on a one-chip semiconductor substrate which serves as a common drain. The respective source regions are commonly connected to the source electrode through source electrode contacts. A gate electrode is formed on the base region through an insulating film. In this case, each source region takes up a very small area on the surface of the semiconductor chip. For this reason, it is very difficult to form source electrode contacts. As a result, the source region must be formed to have a considerably large size, thus degrading the packing density. A sufficient power output cannot be obtained by a semiconductor chip having a limited size, resulting in inconvenience.

Fig. 1 is a plan view showing a conventional power MOSFET. Referring to Fig. 1, projections 12 arranged in a net-like pattern are formed integrally with an n-type semiconductor substrate 11, as indicated by the dashed lines. P-type regions 13 are formed in hexagonal recesses defined and surrounded by the projections 12, respectively. A hexagonal ring-shaped n-type source region 14 is formed at the boundary

between each p-type region 13 and the corresponding projection 12 to have a predetermined width. Each source region 14 is formed between a portion (not shown) slightly toward the corresponding projection 12 from the solid line of the intermediate hexagon, and the alternate long and short dashed line of the smallest hexagon. Areas indicated by the solid lines correspond to gate electrodes 15 forming a net-like pattern, each of which covers the entire area of the corresponding projection 12 and part of the corresponding source region 14 through a gate insulating film.

In the power MOSFET having the structure described above, the source regions 14 respectively surrounded by the projections 12 are independent of each other. The source electrode contacts must be formed on the source regions 14, respectively. The formation of source electrode contacts on the respective source regions 14 may present a problem from the viewpoint of yield of the semiconductor devices. Furthermore, the source regions 14 may not be too much decreased in size in order to form source electrode contacts on the respective source regions 14. Then, the packing density of the prepared power MOSFET cannot be greatly increased. This indicates that a sufficient effective channel width cannot be obtained. As a result, a high power output cannot be obtained. The gate electrode 15 with the net-like pattern is usually formed with polycrystalline silicon which has a gate bonding pad area connected with an aluminum wire used as a taking-out electrode. As a result, wiring between the gate electrode 15 and the bonding pad area is made of polycrystalline silicon with relatively high resistivity, whereby the operating speed cannot be increased.

It is, therefore, an object of the present invention to provide a high-speed, high-power MOSFET which provides a high packing density and a sufficient effective channel width.

In order to achieve the above object of the present invention, there is provided a power MOSFET, comprising: a plurality of projections formed integrally on a semiconductor substrate of one conductivity type which serves as a drain region, each of the plurality of projections having a rectangular surface and a substantially identical size, and the plurality of projections having a plurality of rows of projections arranged in the longitudinal direction thereof and a plurality of columns of projections arranged in the transverse direction thereof which are respectively spaced apart from each other by predetermined distances such that the projections of one of the plurality of rows of projections are offset by a distance corresponding to half of a long side of the rectangular surface with respect to the projections of an adjacent one of the plurality of rows of projections; a base region of another conductivity type formed to cover a surface portion of the semiconductor substrate which excludes surfaces of the plurality of projections; a plurality of source regions of the one conductivity type each of which is formed around the sides of each of the plurality of projections so as to sandwich the base region having a predetermined width therebetween; an insulating film formed to cover surfaces of the plurality of projections, the base region, and the plurality of source regions; a plurality of gate films formed above at least the surfaces of the plurality of projections and the base region via the insulation film; a plurality of source electrode contacts each formed between first and second projections arranged in the row direction of the projections, which are adjacent to each other so as to connect the source region formed around the first projection and the source region formed around the second projection; and a plurality of gate electrode contacts which respectively extend through said insulating film to be connected to the plurality

of gate electrodes.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a plan view of a conventional power MOSFET;

Fig. 2 is a partial plan view of a power MOSFET according to an embodiment of the present invention; and

Fig. 3 is a perspective view showing part of the power MOSFET shown in Fig. 2 taken along the line III - III.

A power MOSFET according to an embodiment of the present invention will be described with reference to Figs. 2 and 3. Referring to Fig. 2, a plurality of projections 22a-1, 22a-2,..., 22b-1, 22b-2,..., and 22c-1, 22c-2,... are formed on the surface of an n-type semiconductor substrate 21 so as to respectively have rectangular surfaces. The projections 22a-1, 22a-2,..., 22c-2,... are of an identical size. They are formed to be spaced apart from each other along their longitudinal direction by a predetermined distance. The projections 22a-1, 22a-2,... are offset from the projections 22b-1, 22b-2,... along their longitudinal direction such that the center of the long side of the rectangular surface of the projection 22b-2, for example, is aligned with the center of an area between the projections 22a-1 and 22a-2. The projections 22c-1, 22c-2,... which are aligned on a row adjacent to the row of the projections 22b-1, 22b-2,... are offset therefrom along their longitudinal direction such that the center of the long side of the rectangular surface of the projection 22c-1, for example, is aligned with the center of an area between the projections 22b-1 and 22b-2.

The surface portion of the semiconductor substrate 21 which excludes the rectangular surfaces of the projections 22a-1, 22a-2,..., 22b-1, 22b-2..., and 22c-1, 22c-2 is covered with a p-type base region 23.

Each projection (e.g., the projection 22a-1) is surrounded by a corresponding base region (e.g., a base region 23a) of a predetermined thickness. The surrounding base region is used as a channel region to be described later. The top surface of the base region 23a used as the channel region is at the same level as the surface of the projection 22a-1. Any other projection 22a-2,... 22b-1,... and 22c-1,... has the same arrangement as the projection 22a-1.

An n^+-type source region 24 is formed around the projection 22a-1 so as to sandwich the base region 23a as the channel region therebetween. The top surface of the source region 24 is at the same level as the top surfaces of the projection 22a-1 and the base region 23a.

The projection 22a-2 adjacent to the projection 22a-1 is surrounded by a base region 23b. An source region 24 is also formed around the base region 23b. A source electrode contact 25a is formed between the projections 22a-1 and 22a-2 so as to commonly connect the source regions 24. In practice, the top surfaces of base regions 23a,..., 23g,... which are formed around the projections 22a-1,..., 22c-1,..., and the top surfaces of the projections 22a-1,..., 22c-1,... are covered by a gate region through a gate insulating film. Gate electrodes and source electrodes are deposited through the insulating film, thereby completing a power MOSFET.

The internal structure and the arrangement of the gate and source electrodes of the power MOSFET of this embodiment will be described with reference to Fig. 3. Referring to Fig. 3, the n-type semiconductor substrate 21 comprises an n^+-type substrate drain 21a and an n-type epitaxial drain 21b formed thereon. The lower surface of the substrate drain 21a is entirely covered by a drain electrode 31. The projections 22a-1,..., 22b-1,..., and 22c-1,... are formed integrally with the

epitaxial drain 21b. The surface of the epitaxial drain 21b is covered with the p-type base region 23. The projections 22a-1 and 22c-1 are surrounded by part of the base region 23 which is used as the channel regions 23a and 23c.

The source region 24 is formed around the projection 22a-1 through the channel region 23a.

In practice, in one case of manufacturing a power MOSFET, the n-type epitaxial drain 21b is uniformly formed on the surface of the substrate drain 21a to have a uniform thickness so as to correspond to the thickness of each of the projections 22a-1,..., 22c-2,.... Thereafter, a photoresist pattern is formed on the projections 22a-1,... and is used as a mask for doping the exposed portions with a p-type impurity, thereby forming the p-type base region 23. Furthermore, using a proper mask, source regions 24,... may be formed on the surface layer of the base region 23. Therefore, the top surfaces of the projections 22a-1,... are readily found to be at the same level as those of the channel regions 23a,... and the source regions 24,....

A silicon oxide film 32 is then formed to cover the entire surfaces of the projections 22a-1,..., the base region 23, and the source regions 24,.... A plurality of polycrystalline silicon gate films 33a, 33b,... which respectively correspond to the projections 22a-1,... are formed in the silicon oxide film 32. The polycrystalline silicon gate film 33a is formed to oppose the top surfaces of the projection 22a-1 and the channel region 23a so as to sandwich the oxide film 32 therebetween. Other polycrystalline silicon gate films 33b,... are formed in a similar manner. Contact holes are formed in the oxide film 32 which is formed over the gate films 33c, 33e and 33d. Gate electrode contacts 33c-1, 33d-1 and 33e-1 are formed in the oxide film 32 through the respective contact holes.

The gate electrode contacts 33c-1, 33d-1 and 33e-1 are commonly connected to a gate electrode 34 which is formed on the oxide film 32 so as to extend across the projections 22a-2, 22b-2 and 22c-2 (Fig. 2).

A source electrode contact hole 35 is formed in a portion between the projections 22a-1 and 22a-2. The contact hole 35 is formed by selectively etching the oxide film 32, such that one end of each of source regions 24 respectively formed around the projections 22a-1 and 22a-2 are exposed through the contact hole 35. At this time a portion 26a (Fig. 2) of the base region 23 is also exposed through the contact hole 35. A metal such as aluminum is deposited in the contact hole 35 so as to electrically connect the source regions 24, thereby forming a source electrode contact 25a. The portion 26a is connected to the contact 25a to short circuit the base region 23. Similarly, a source electrode contact 25d is formed between the projections 22c-1 and 22c-2. The source electrode contacts 25a, 25d formed so as to sandwich one of the projections (e.g., 22b-2 in Fig. 2) therebetween in a direction perpendicular to the long side of each projection, are commonly connected to a source electrode 36.

Two source electrodes are formed along two lines which are shifted by a distance corresponding to half of the long side of each projection 22a-1,..., 22c-2,... with respect to the line connecting the source electrode contacts 25a and 25d. The source electrode contact 25b is connected to one of the source electrodes (not shown), and the source electrode contact 25c is connected to the other of the source electrodes. Fig. 3 only illustrates a source electrode 37 which is connected to the source electrode contact 25c.

With the above arrangement, a distance between the projections 22a-1 and 22a-2 can be determined so as to readily form the source electrode contact 25a.

Furthermore, the size of the source electrode contact 25a does not adversely affect the effective channel width of the channel region 23a formed between the drain region of the projection 22a-1 and the source region 24. Therefore, the substrate area can be effectively utilized while the effective channel width can be sufficiently wide, thereby increasing the packing density of the power MOSFET. Since, the respective polycrystalline silicon gate electrodes are connected to the gate aluminum wiring electrode 34, the value of the gate resistance may be made very small compared with the conventional power MOSFET, thereby realizing a high operation speed.

For example, a power MOSFET having the structure of the embodiment shown in Figs. 2 and 3 was formed on a chip having dimensions of 5.5 mm × 5.5 mm. In this case, the length L1 and width L2 of the respective projections 22a-1,..., 22c-2,... are 200 μm, and 27 μm, respectively. An effective channel width of the power MOSFET was 114 cm, and a gate resistance thereof was 0.3 ohm. On the other hand, a conventional power MOSFET was formed on a chip having the same dimensions as those described above. An effective channel width of the conventional power MOSFET was 93 cm, and a gate resistance thereof was 1.7 ohms. As a result, it is found that the power MOSFET according to the present invention has a wide effective channel width, a small gate resistance and a high power with a high operation speed.

Furthermore, as can be seen in Fig. 2, since the four source regions 24 formed around the projections 22a-1, 22b-1, 22b-2 and 22c-1 are commonly connected through the single source electrode contact 25b, for example, the yield of the power MOSFETs is greatly increased, thus contributing to an increase in the packing density of the device.

In operation, when predetermined voltages are

applied to the drain electrode 31, the source electrodes 36 and 37, and the gate electrode 34, a current I flows from the epitaxial drain 21b to all the projections 22a-1,..., 22c-1,... as shown in Fig. 3. The current I further flows in the source regions 24 from the side surfaces of all the projections through the channel regions 23a, 23b,.... This operation is similar to the conventional power MOSFET, and a detailed description thereof will be omitted.

In the above embodiment, the semiconductor substrate drain 21 is of n-type, and the source region is of n^+-type. However, the substrate may comprise a p-type semiconductor substrate, and the source region may comprise a p^+-type source region.

Claims:

1. A power MOSFET having a semiconductor substrate used as a common drain region, a base region for dividing a surface of said semiconductor substrate into a plurality of small regions, and a plurality of source regions opposing said drain region through said base region, characterized in that said power MOSFET comprises:

a plurality of projections (22a-1, 22a-2) formed integrally on the surface of said semiconductor substrate (21) of one conductivity type which serves as said drain region, each of said plurality of projections having a rectangular surface, and said plurality of projections having a plurality of rows of projections and a plurality of columns of projections which are respectively spaced apart from each other by predetermined distances such that said projections (22a-1, 22a-2) of one of said plurality of rows of projections are offset by a distance corresponding to half of a long side of said rectangular surface with respect to said projections (22b-1, 22b-2) of an adjacent one of said plurality of rows of projections;

a base region (23) of another conductivity type formed to cover a surface portion of said semiconductor substrate (21) which excludes surfaces of said plurality of projections (22a-1, 22a-2);

a source region (24) of said one conductivity type which is formed to surround said plurality of projections (22a-1, 22a-2) so as to sandwich said base region (23a, 23b) having a predetermined width therebetween;

an insulating film (32) formed to cover surfaces of said plurality of projections (22a-1, 22a-2), said base region (23), and said source region (24);

a plurality of gate films (33a - 33e) formed on at least said surfaces of said plurality of projections

(22a-1, 22a-2) and said base region (23a, 23b) and which are formed on said insulating film (32);

a plurality of source electrode contacts (25a) formed such that each of said source electrode contacts is formed between first and second projections (22a-1, 22a-2) of said plurality of projections which are longitudinally adjacent to each other so as to connect said source region (24) respectively formed around said first projection (22a-1) and said second projection (22a-2); and

a plurality of gate electrode contacts (33c-1, 33d-1, 33e-1) which respectively extend through said insulating film (32) to be connected to said plurality of gate films (33a - 33e).

2. A power MOSFET according to claim 1, characterized in that said semiconductor substrate (21) comprises an n^+-type substrate drain (21a) and an n-type epitaxial drain (21b) formed on said n^+-type substrate drain (21a), said plurality of projections (22a-1, 22a-2) being formed in a surface layer of said n-type epitaxial drain (21b).

3. A power MOSFET according to claim 1, characterized in that said gate films (33a - 33e) comprise polycrystalline silicon films.

4. A power MOSFET according to claim 1, characterized in that said semiconductor substrate comprises a p^+-type substrate drain and a p-type epitaxial drain formed on said p^+-type substrate drain, said plurality of projections being formed in a surface of said p-type epitaxial drain.

FIG. 1

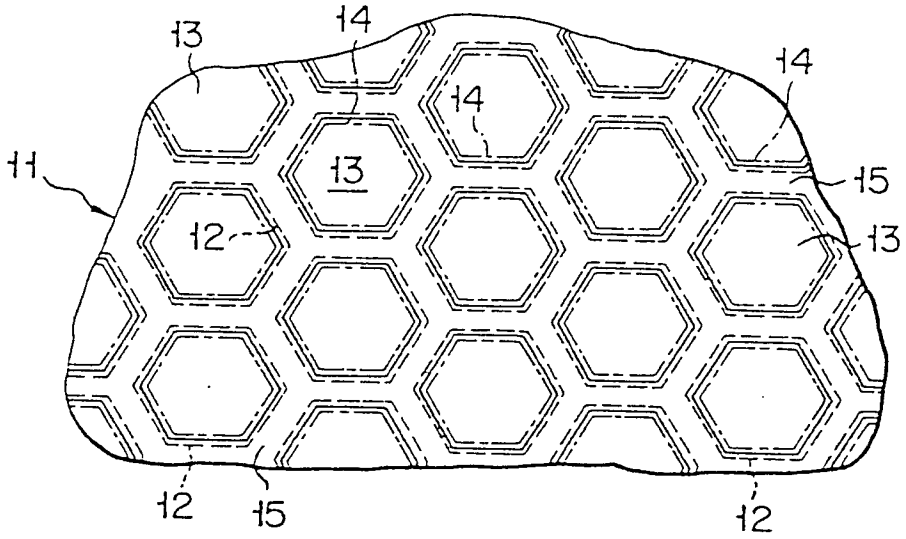
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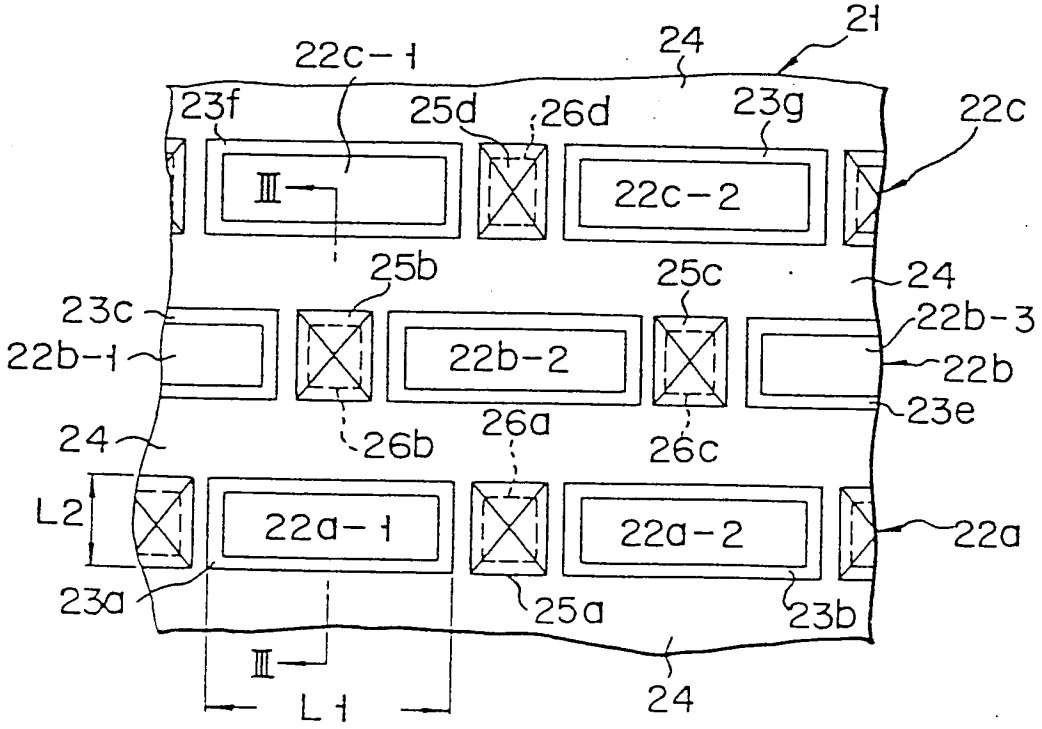
FIG. 2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22b-2
22b
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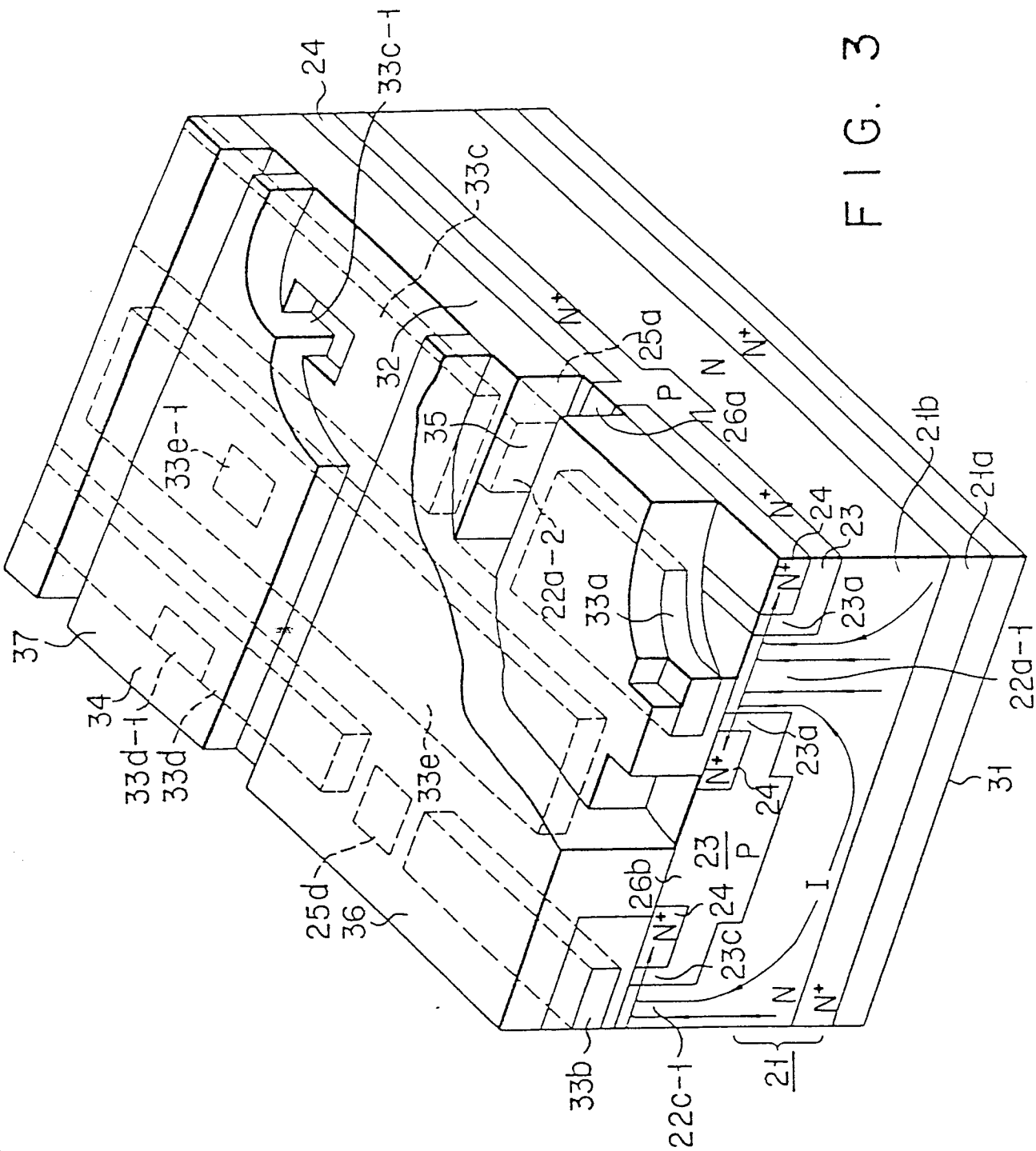
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23a
22a-2
33a
22a-1
37
34
33d-1
33d
33e
31
25d
36
26b
N+
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P
23a
N+
24
23c
I
N
N+
33b
22c-1
21

FIG. 3

(E1

European Patent Office

EUROPEAN SEARCH REPORT

0091079
Application number

EP 83 10 3132

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. ³)
A	US-A-4 148 046 (HONEYWELL INC.) * Claims 30,40 *	1	H 01 L 29/78 H 01 L 29/08
A	IEEE SPECTRUM, vol. 18, no. 1, January 1981, pages 64-65, New York, USA "Advances in extending performance of power MOS field-effect transistors promise to extend their usefulness..." * Figure *		

TECHNICAL FIELDS SEARCHED (Int. Cl. ³)

H 01 L 29/78
H 01 L 29/08

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	28-08-1983	VANCRAEYNEST F.H.

CATEGORY OF CITED DOCUMENTS

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